FIG. 1

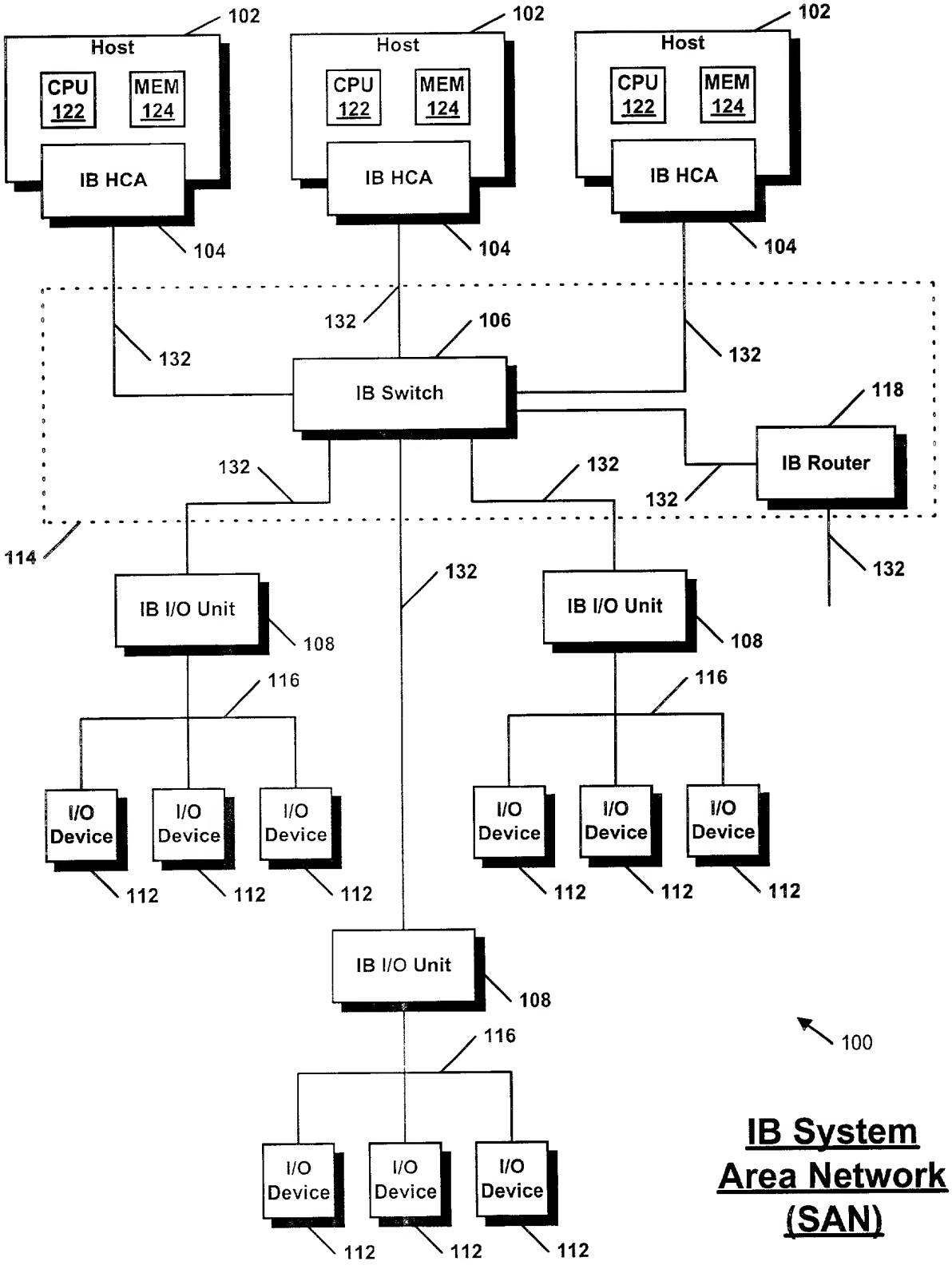
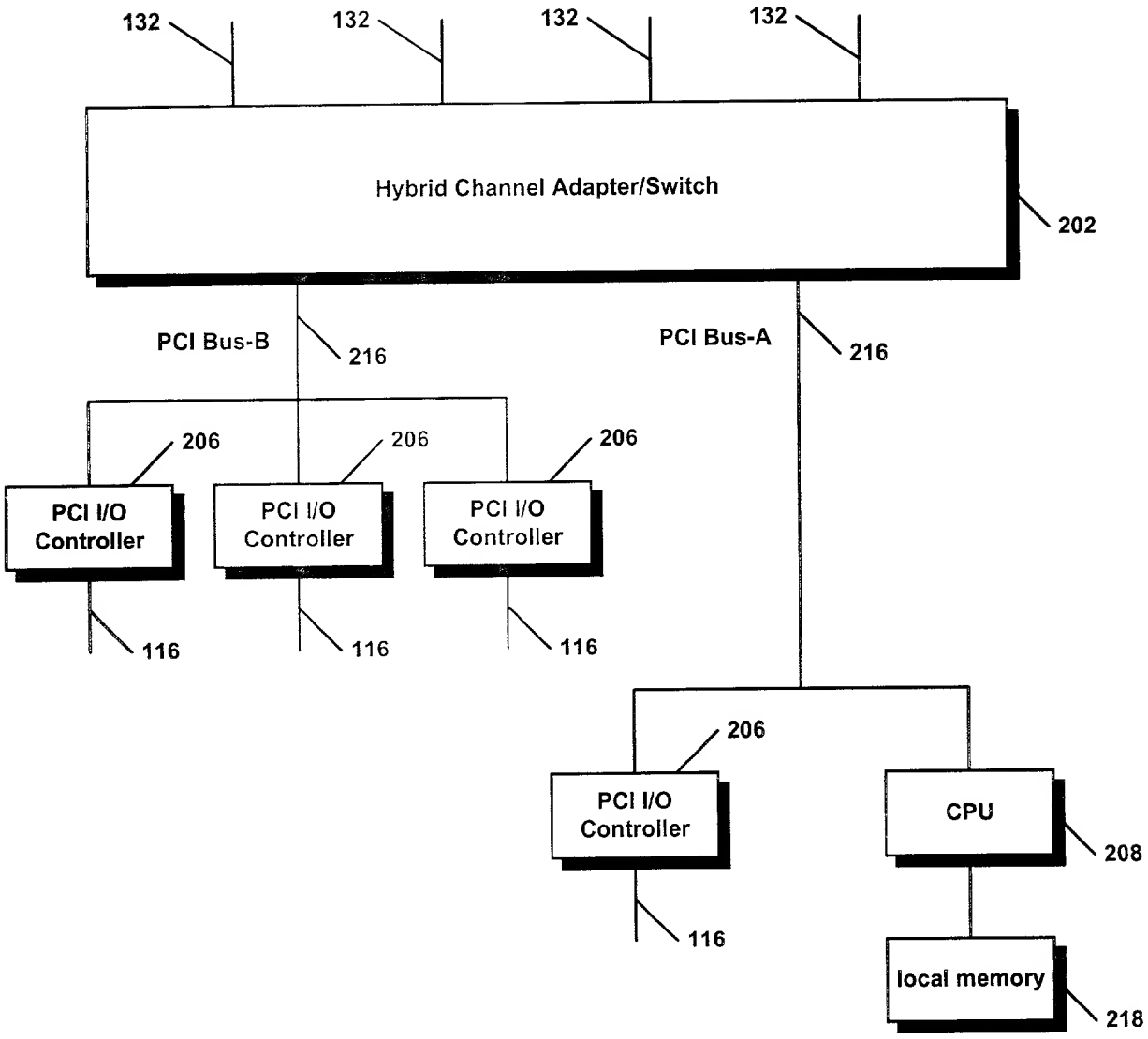
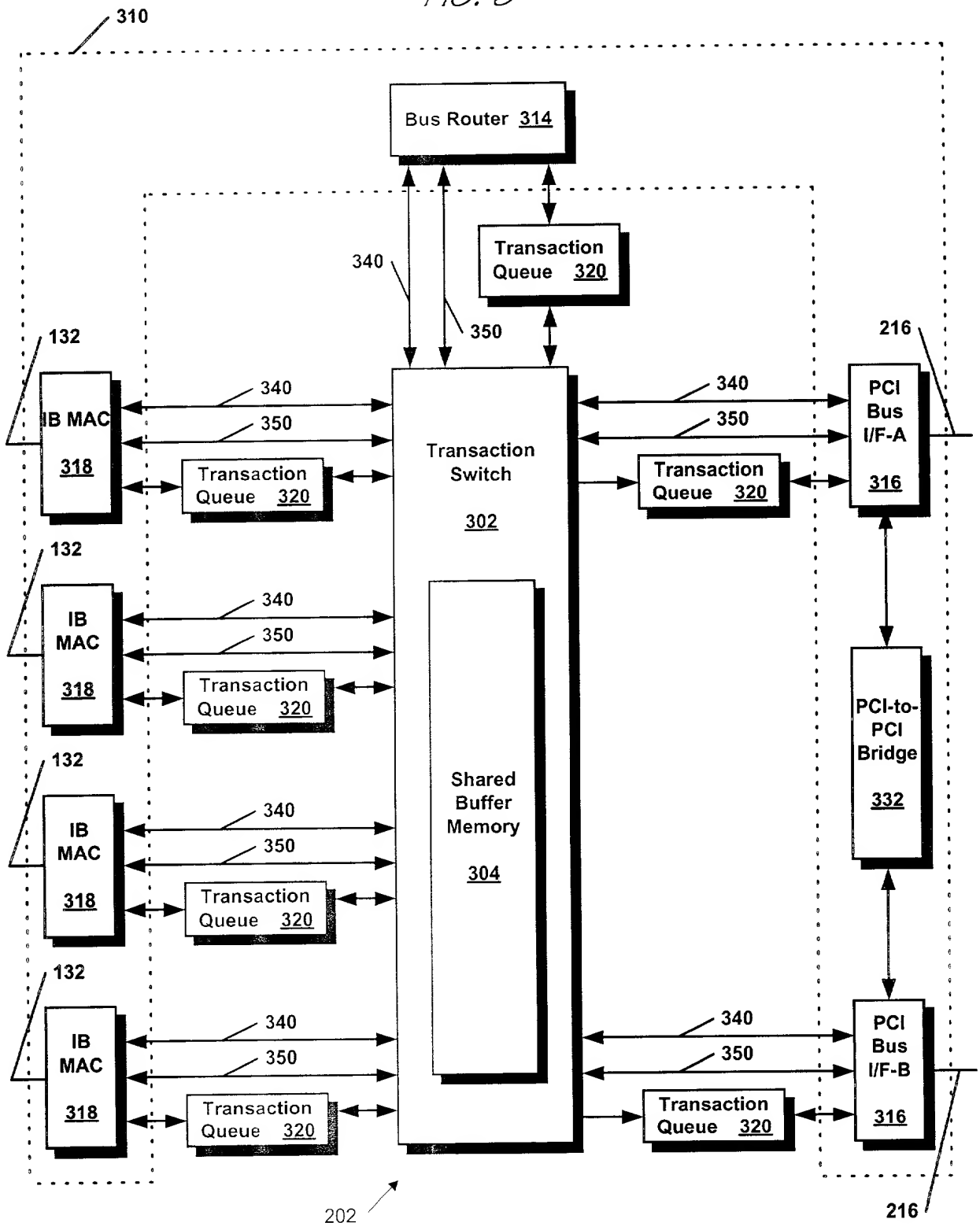

Host
CPU 122
MEM 124
IB HCA
102
104
132
106
IB Switch
118
IB Router
114
IB I/O Unit
108
116
I/O Device
112
100
IB System Area Network (SAN)

FIG. 2



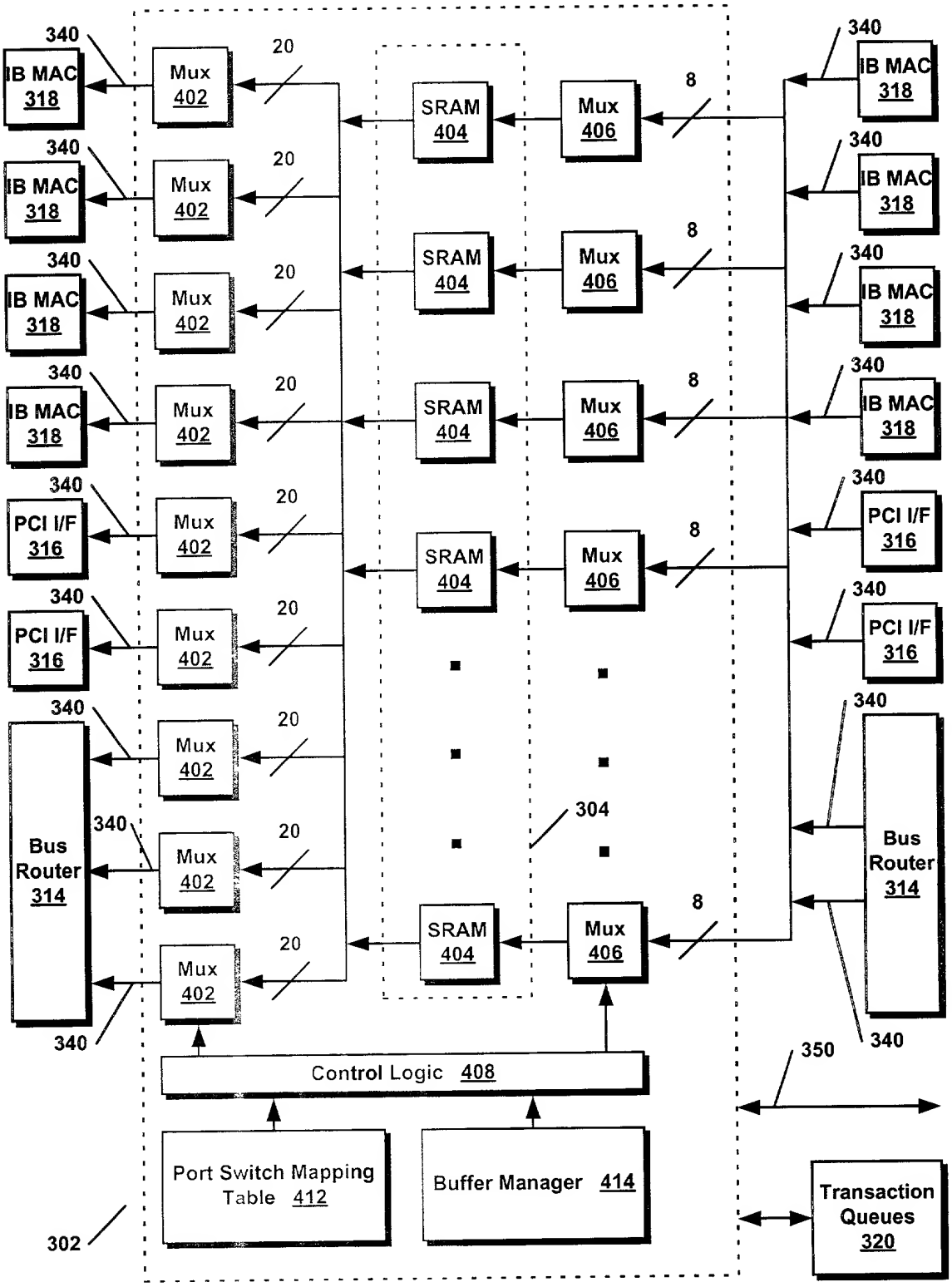
IB Hybrid Channel Adapter/Switch

FIG. 3



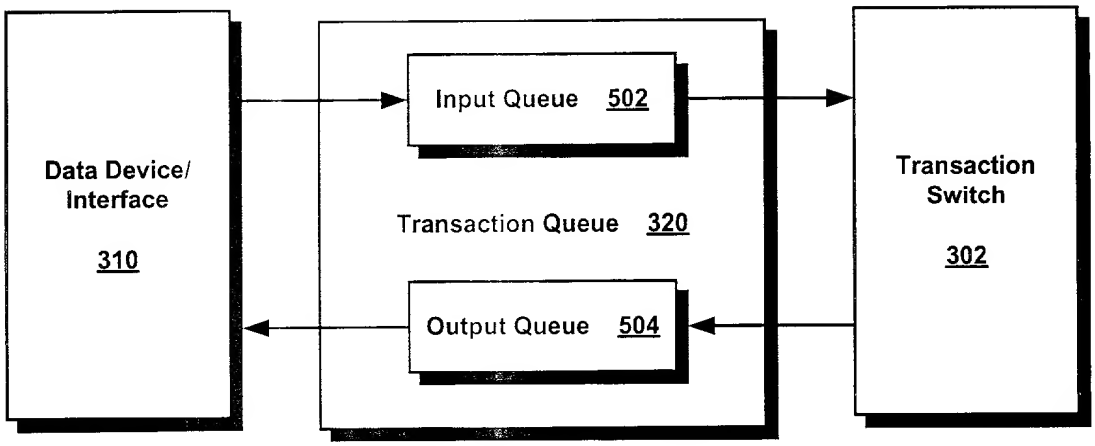
IB Hybrid CA/Switch with Transaction Switch and Shared Buffer Memory

FIG. 4



Transaction Switch Data Paths

FIG. 5



Transaction Queues

FIG. 6

DLID 602	Frame Error 604	LNH 606	Destination QP 608	Packet Length 612	VL 614	Buffer Address 616

MAC Input Queue Entry 600

FIG. 7

Tag 702	PCI Address/Port 704	Length 706	Offset 708	VL 712	Type 714	Buffer Address 716

Bus Router Input Queue Entry 700

FIG. 8

Not Raw 802	Tag 804	Packet Length 806	VL 808	Buffer Address 812

MAC Output Queue Entry 800

FIG. 9

Port 902	Frame Error 904	LNH 906	Destination QP 908	Length 912	VL 914	Buffer Address 916

Bus Router Output Queue Entry 900

FIG. 10

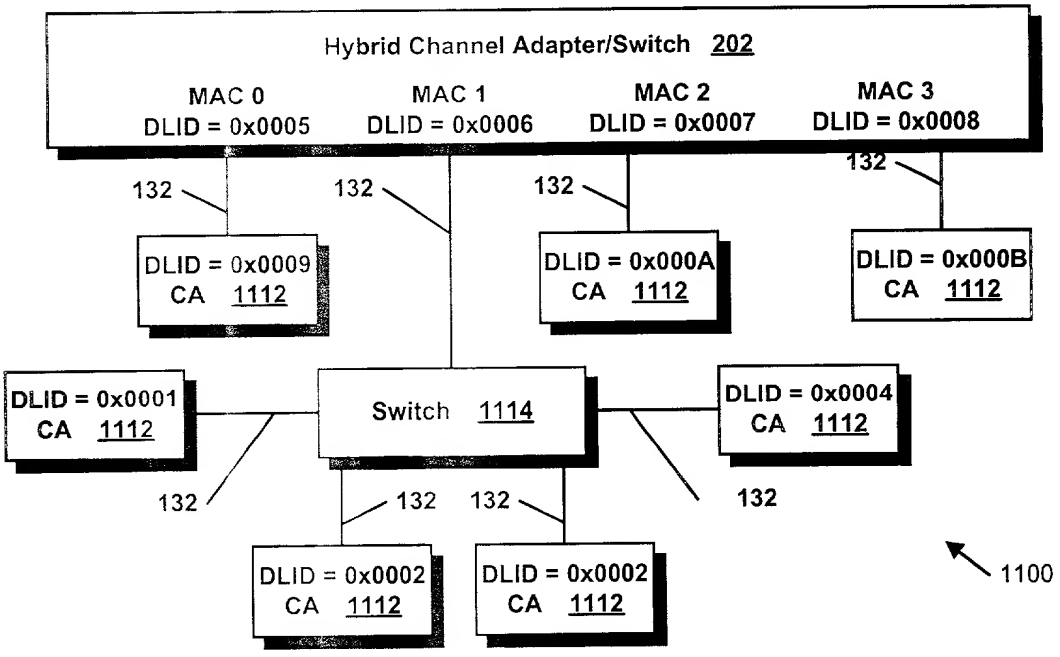
Tag 1002	PCI Address 1004	Length 1006	Offset 1008	PCI Type 1012	Buffer Address 1014

PCI Output Queue Entry 1000

FIG. 11

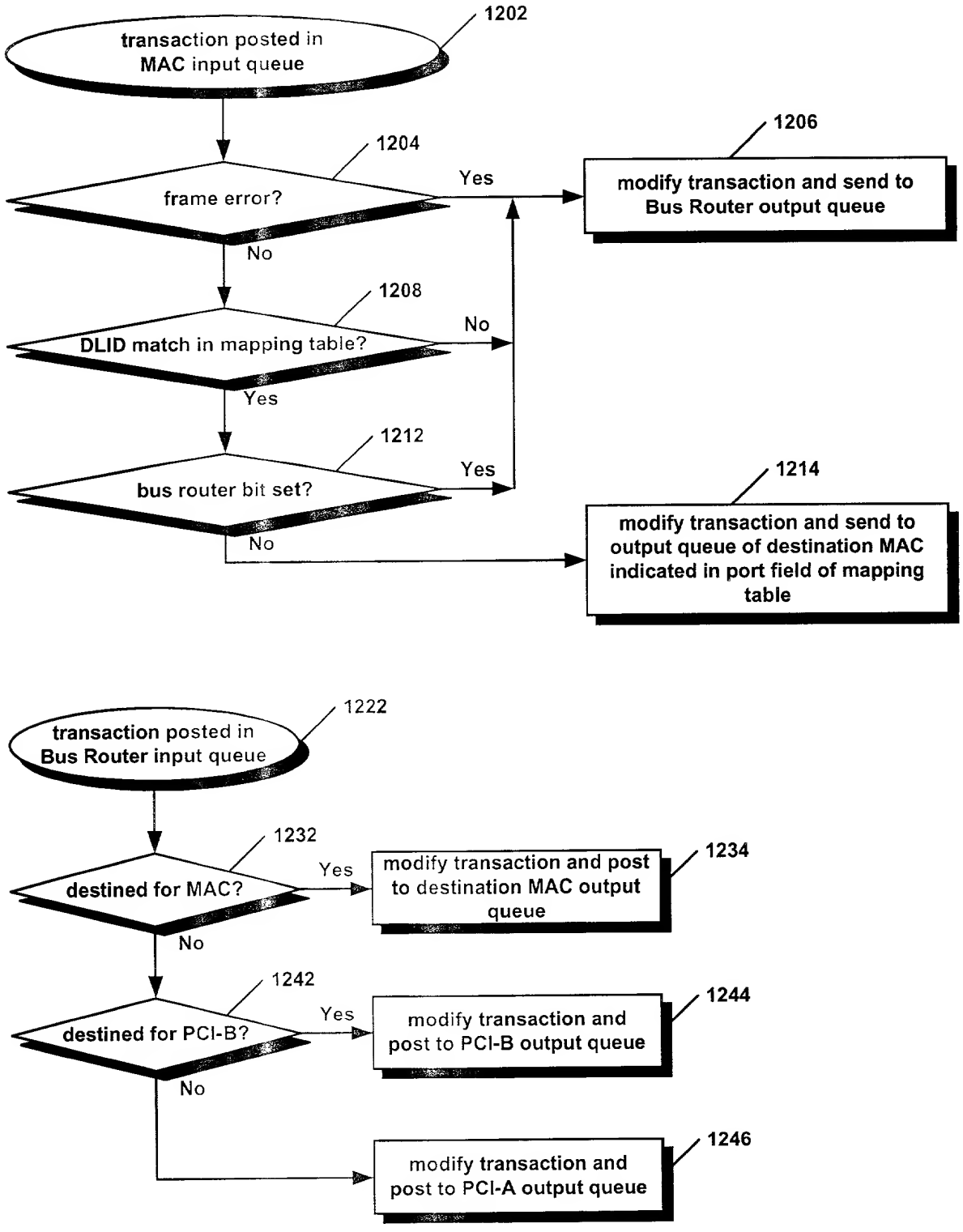
	Bus Router 1102	Port 1104	DLID 1106	Valid 1108
0	1	0	0x0005	1
1	1	1	0x0006	1
2	1	2	0x0007	1
3	1	3	0x0008	1
4	0	1	0x0001	1
5	0	1	0x0002	1
6	0	1	0x0003	1
7	0	1	0x0004	1
8	0	0	0x0009	1
9	0	2	0x000A	1
10	0	3	0x000B	1
11	0	2	-	0
12	0	1	-	0
13	0	3	-	0
14	0	2	-	0
15	0	2	0x0007	1

412



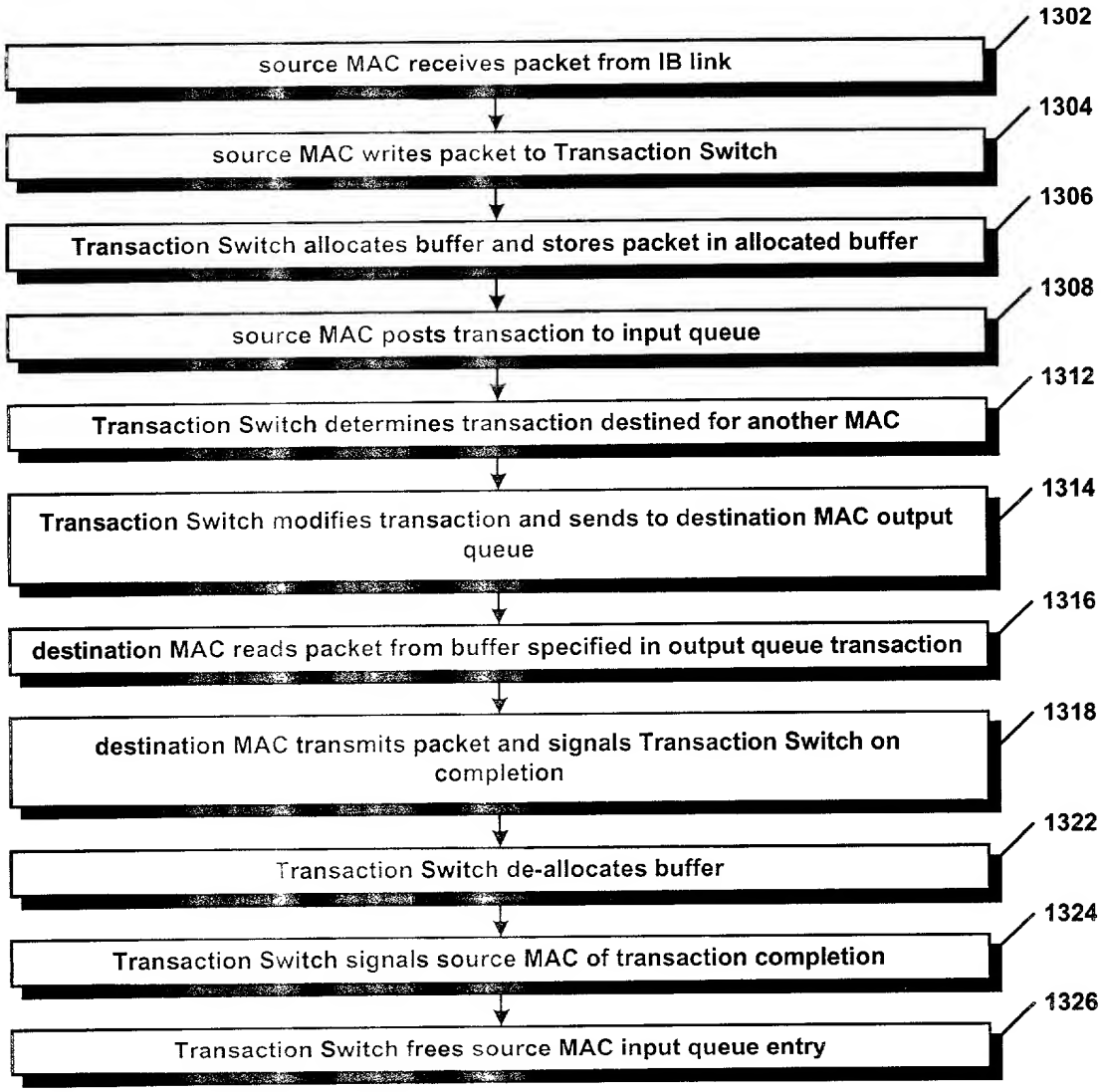
Port Switch Mapping Table in Example Network

FIG. 12



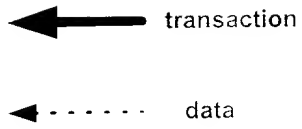
Transaction Switching

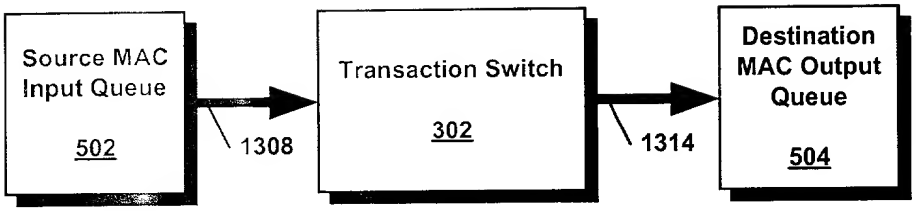
FIG. 13a

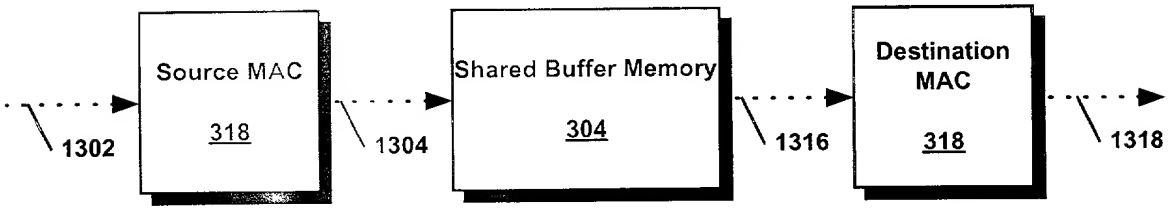


Packet Switching Operation

FIG. 13b

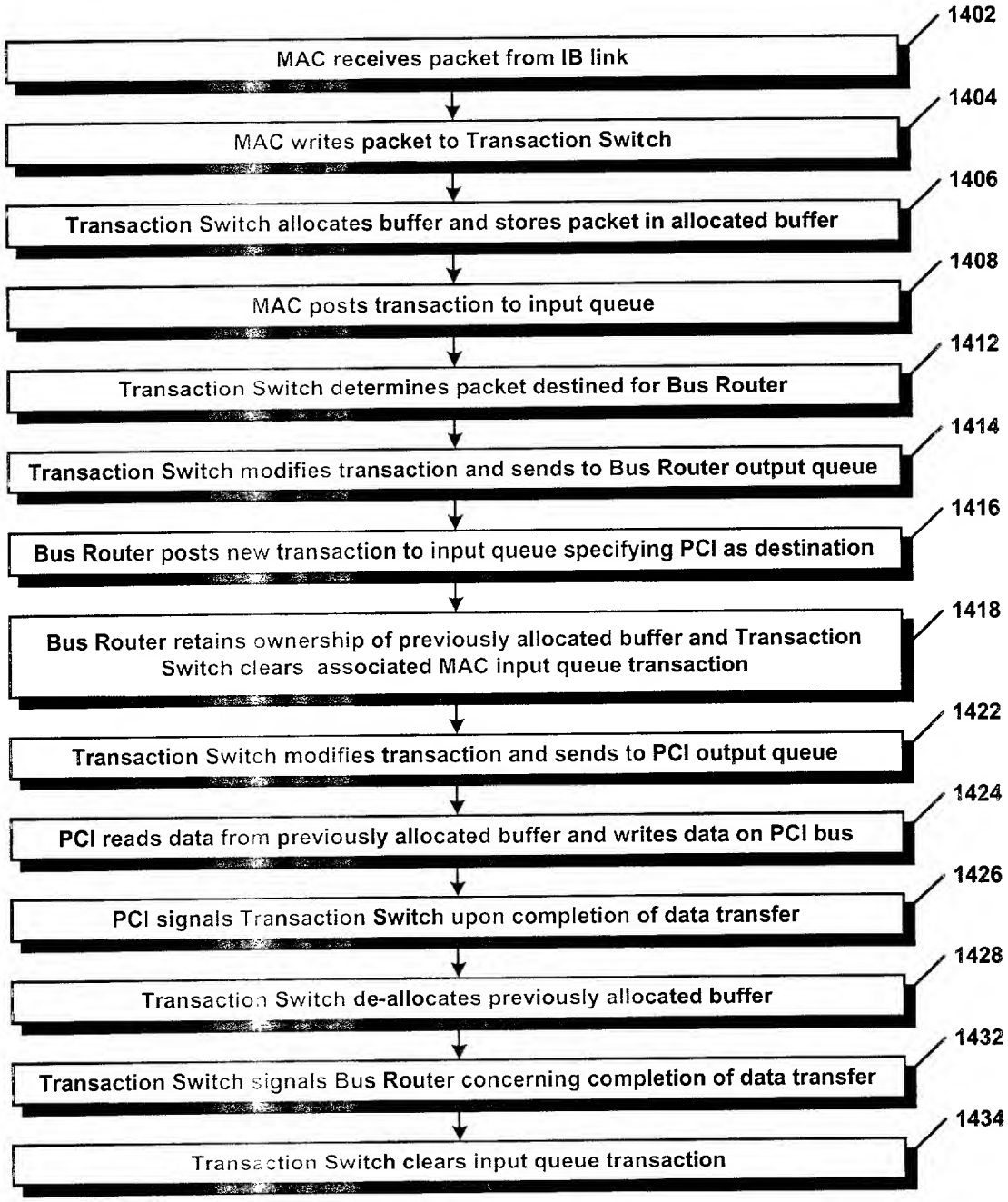






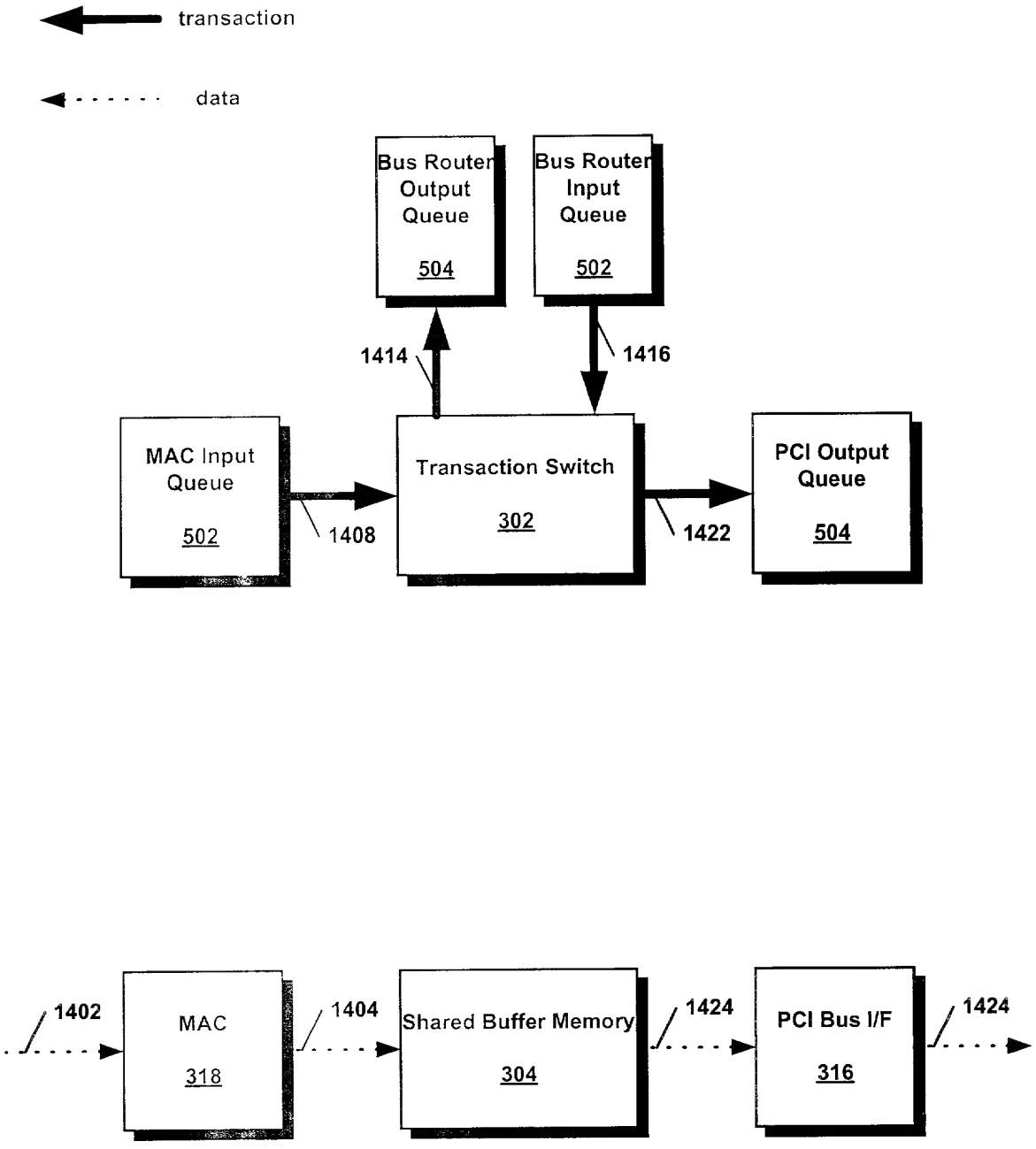
Packet Switching Operation

FIG. 14a



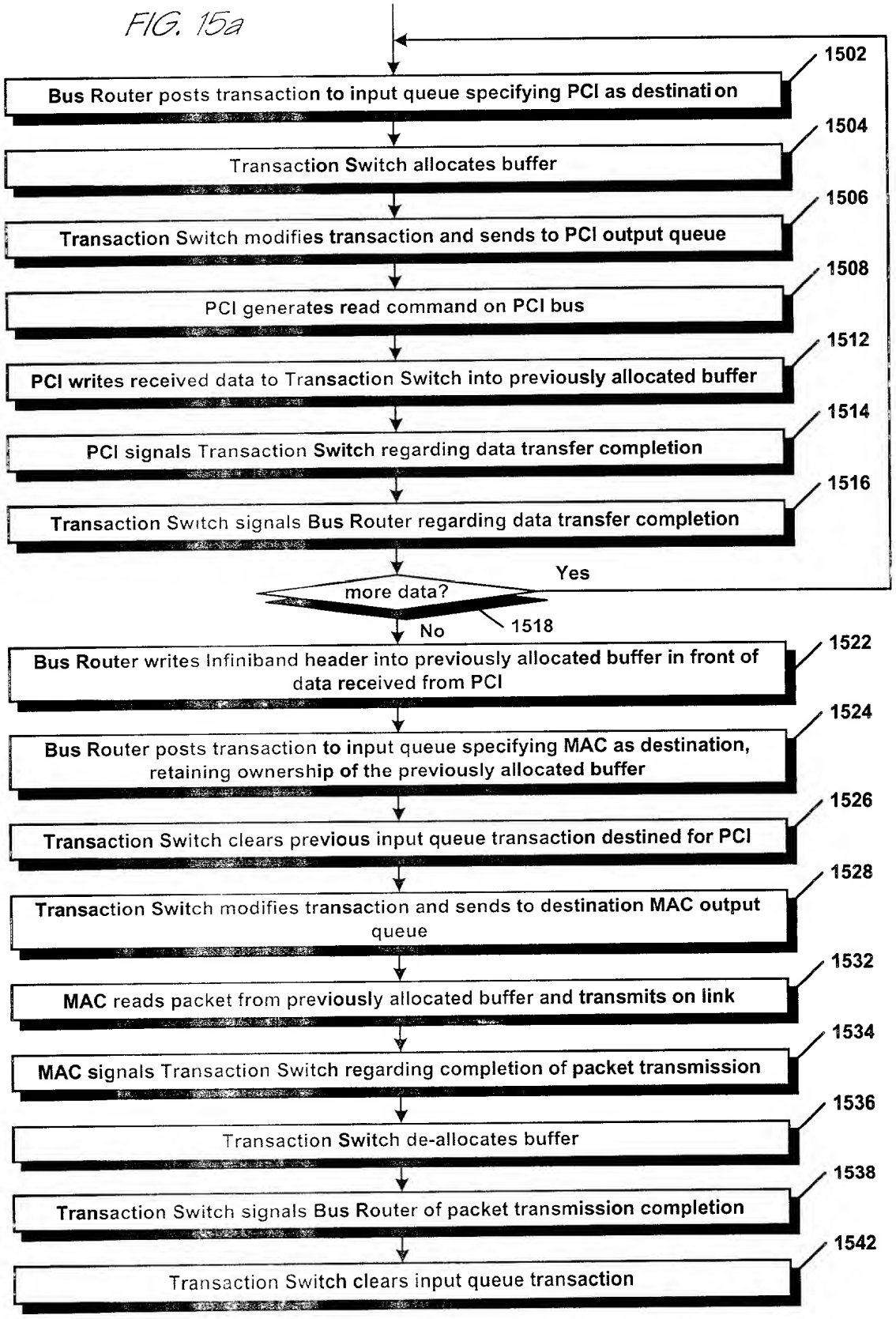
Packetized Data to Addressed Data Operation

FIG. 14b



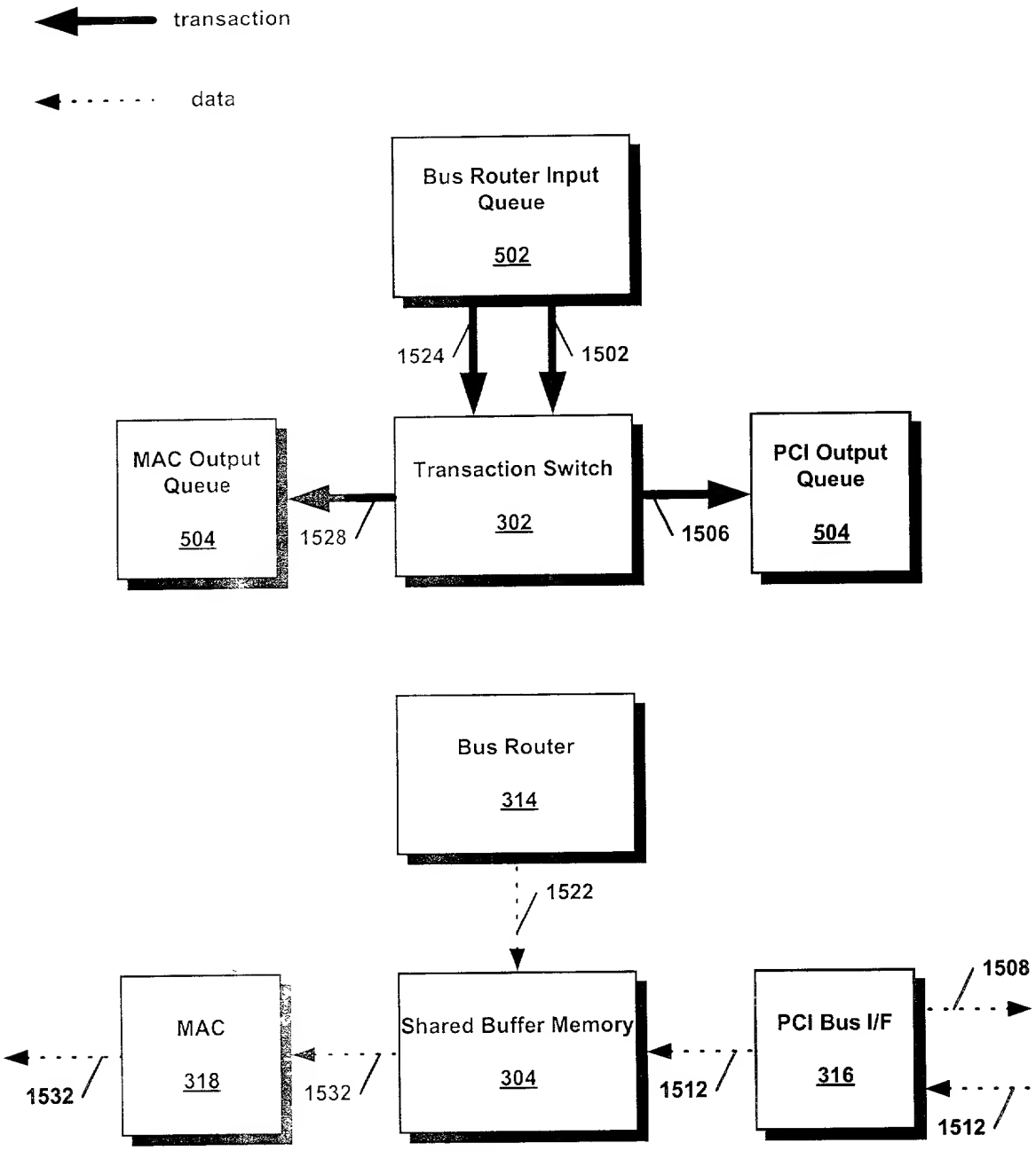
Packetized Data to Addressed Data Operation

FIG. 15a



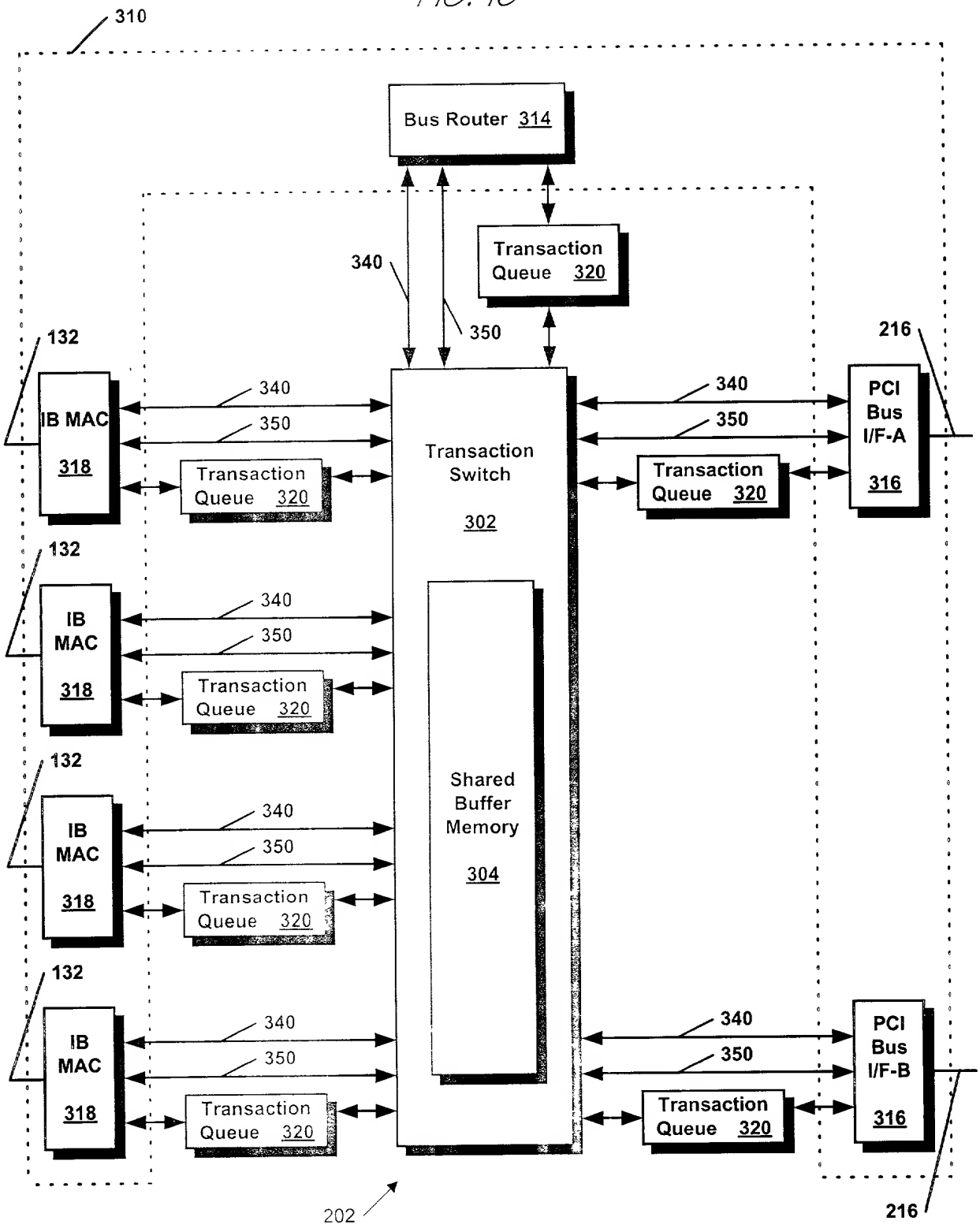
Addressed Data to Packetized Data Operation

FIG. 15b



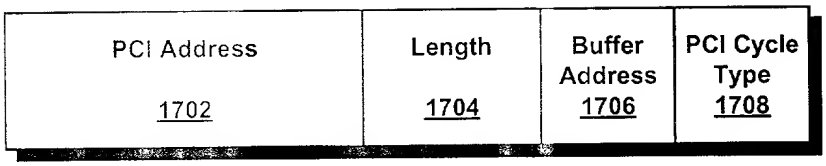
Addressed Data to Packetized Data Operation

FIG. 16



IB Hybrid CA/Switch with Transaction Switch and Shared Buffer Memory

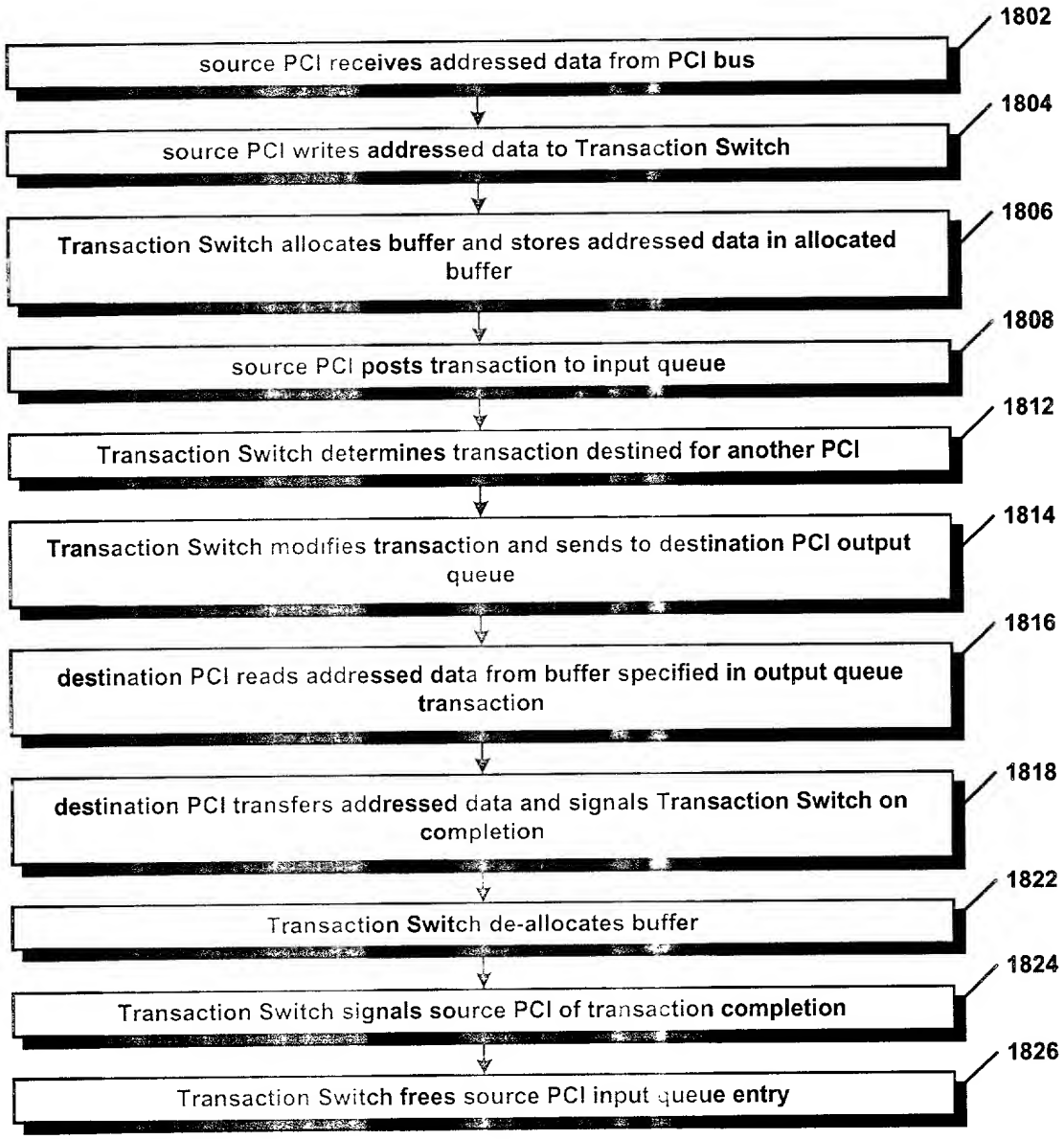
FIG. 17



1700

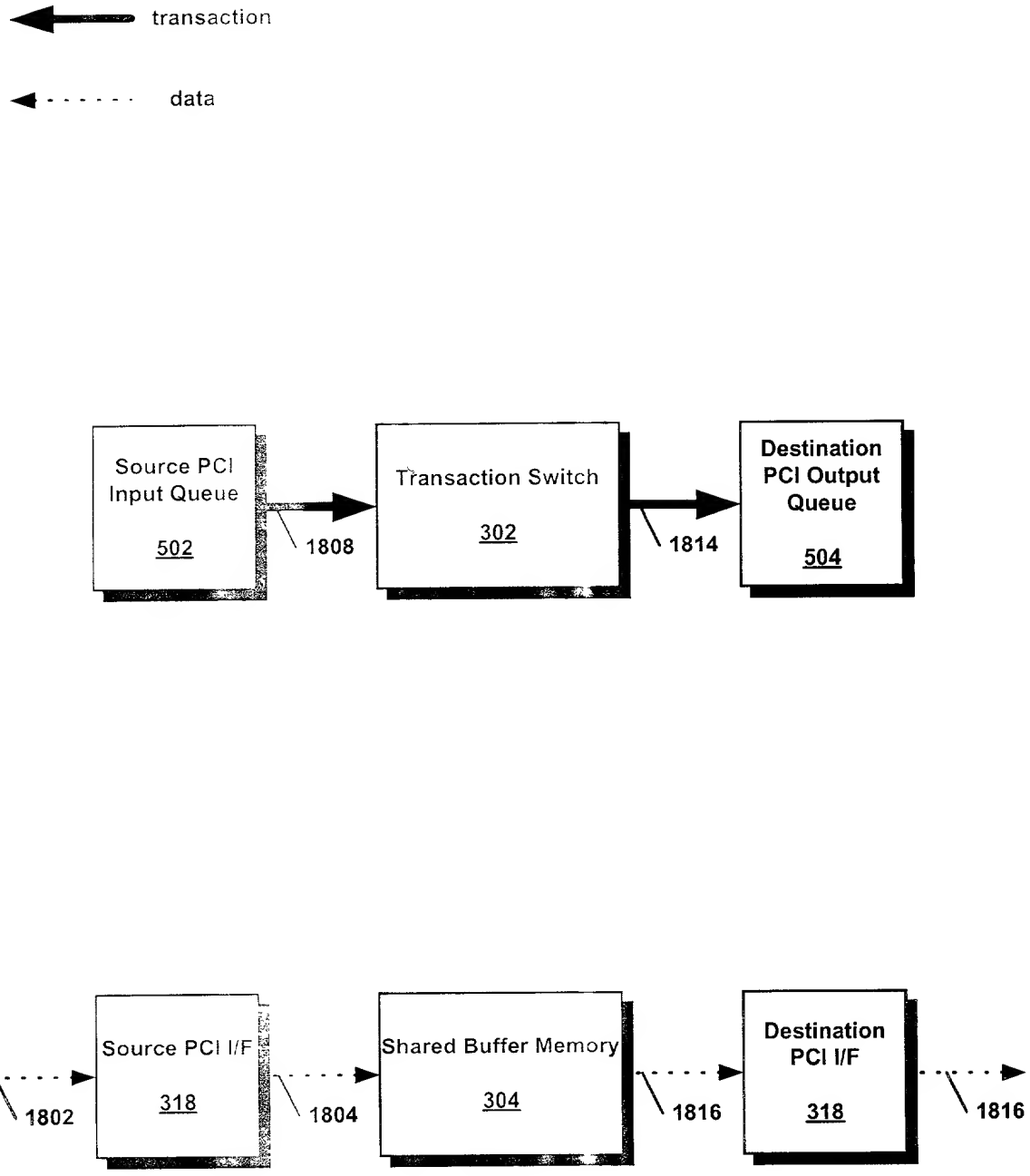
PCI Input Queue Entry

FIG. 18a



Addressed Data Switching Operation

FIG. 18b



Addressed Data Switching Operation